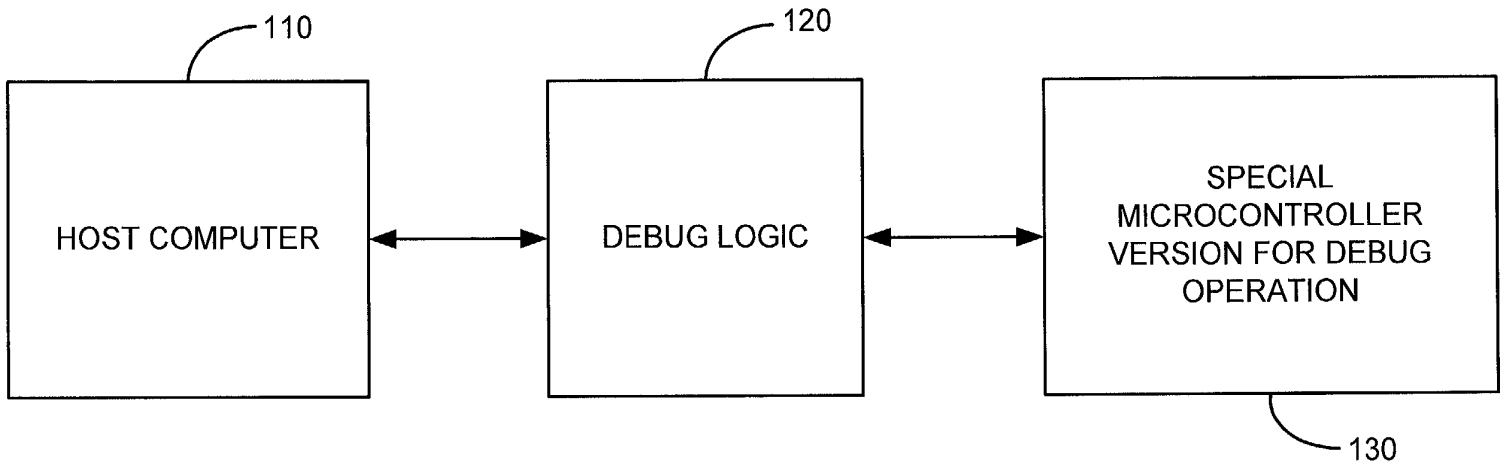

110
120
HOST COMPUTER
DEBUG LOGIC
SPECIAL MICROCONTROLLER VERSION FOR DEBUG OPERATION
130
100
(PRIOR ART)

FIG. 1

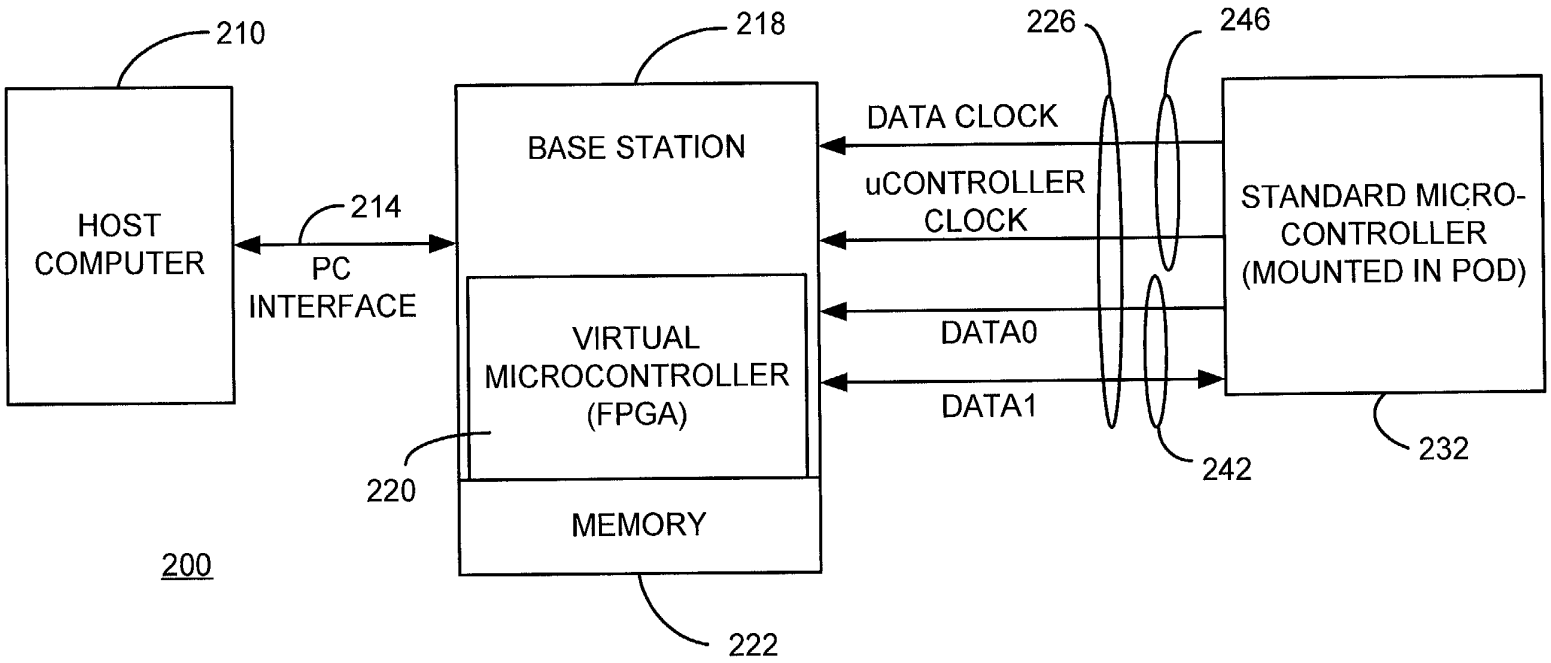

210
218
226
246
HOST COMPUTER
214
PC INTERFACE
BASE STATION
VIRTUAL MICROCONTROLLER (FPGA)
220
MEMORY
222
200
DATA CLOCK
uCONTROLLER CLOCK
DATA0
DATA1
242
STANDARD MICRO-CONTROLLER (MOUNTED IN POD)
232

FIG. 2

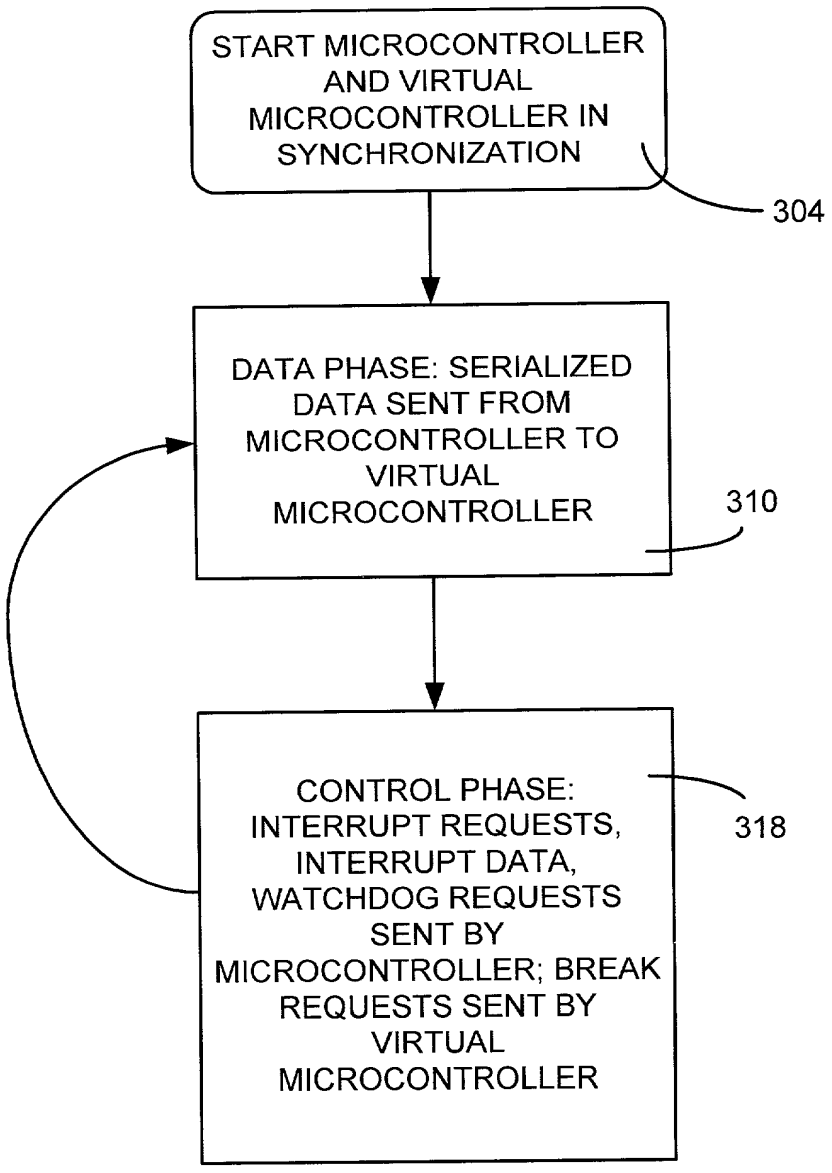
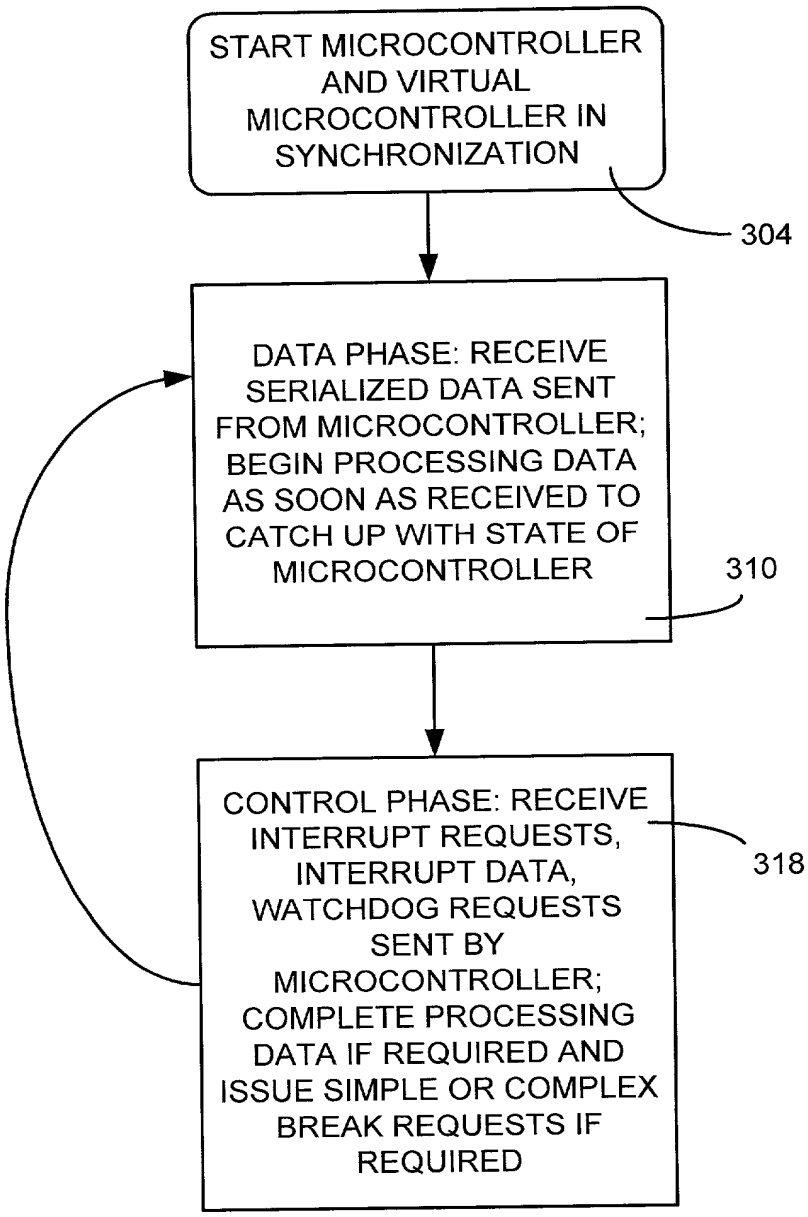

START MICROCONTROLLER AND VIRTUAL MICROCONTROLLER IN SYNCHRONIZATION
304
DATA PHASE: SERIALIZED DATA SENT FROM MICROCONTROLLER TO VIRTUAL MICROCONTROLLER
310
CONTROL PHASE: INTERRUPT REQUESTS, INTERRUPT DATA, WATCHDOG REQUESTS SENT BY MICROCONTROLLER; BREAK REQUESTS SENT BY VIRTUAL MICROCONTROLLER
318

FIG. 3

FIG. 4


START MICROCONTROLLER AND VIRTUAL MICROCONTROLLER IN SYNCHRONIZATION
304
DATA PHASE: RECEIVE SERIALIZED DATA SENT FROM MICROCONTROLLER; BEGIN PROCESSING DATA AS SOON AS RECEIVED TO CATCH UP WITH STATE OF MICROCONTROLLER
310
CONTROL PHASE: RECEIVE INTERRUPT REQUESTS, INTERRUPT DATA, WATCHDOG REQUESTS SENT BY MICROCONTROLLER; COMPLETE PROCESSING DATA IF REQUIRED AND ISSUE SIMPLE OR COMPLEX BREAK REQUESTS IF REQUIRED
318

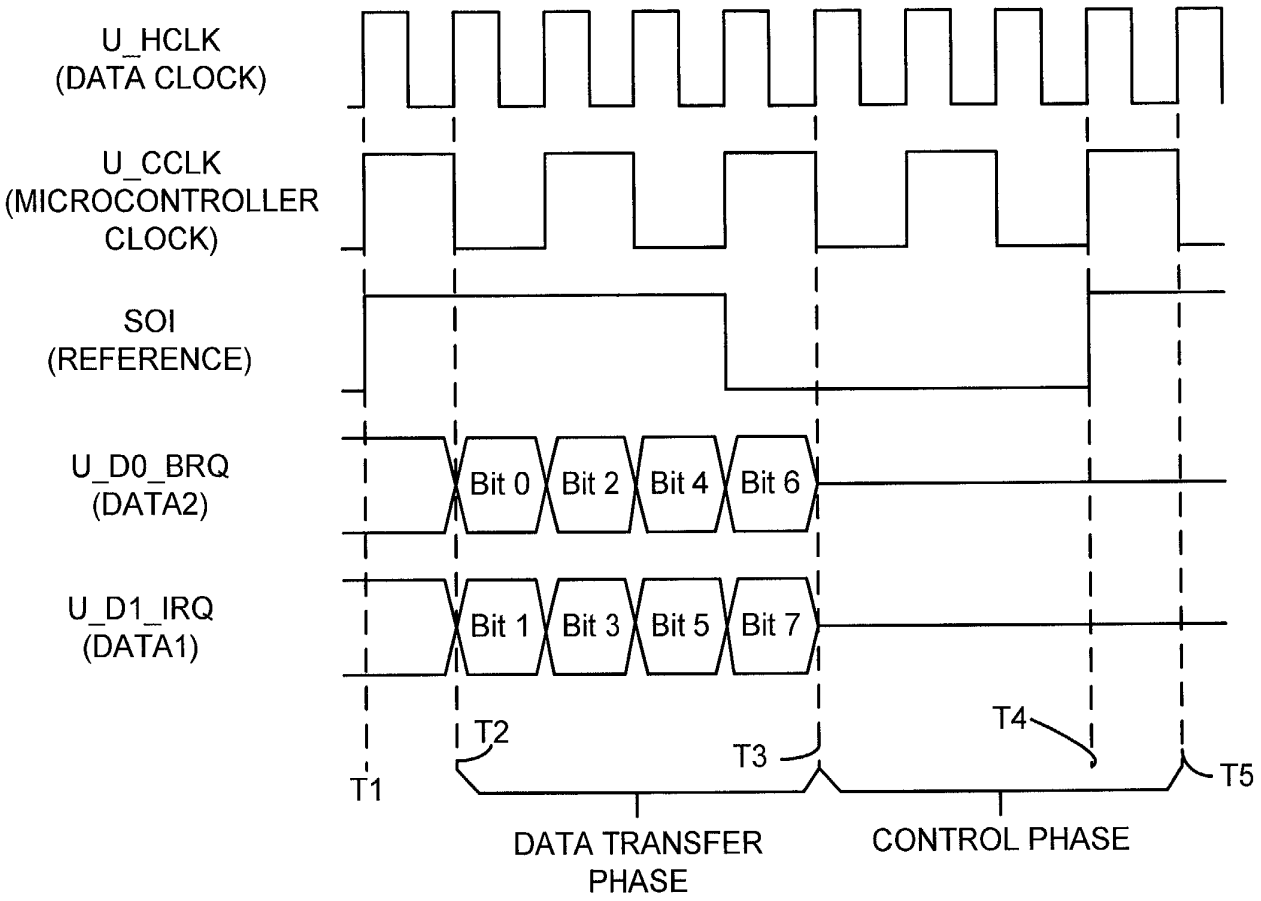

U_HCLK
(DATA CLOCK)
U_CCLK
(MICROCONTROLLER
CLOCK)
SOI
(REFERENCE)
U_D0_BRQ
(DATA2)
U_D1_IRQ
(DATA1)
Bit 0
Bit 2
Bit 4
Bit 6
Bit 1
Bit 3
Bit 5
Bit 7
T1
T2
T3
T4
T5
DATA TRANSFER
PHASE
CONTROL PHASE

FIG. 5

TOBOTF 8218002

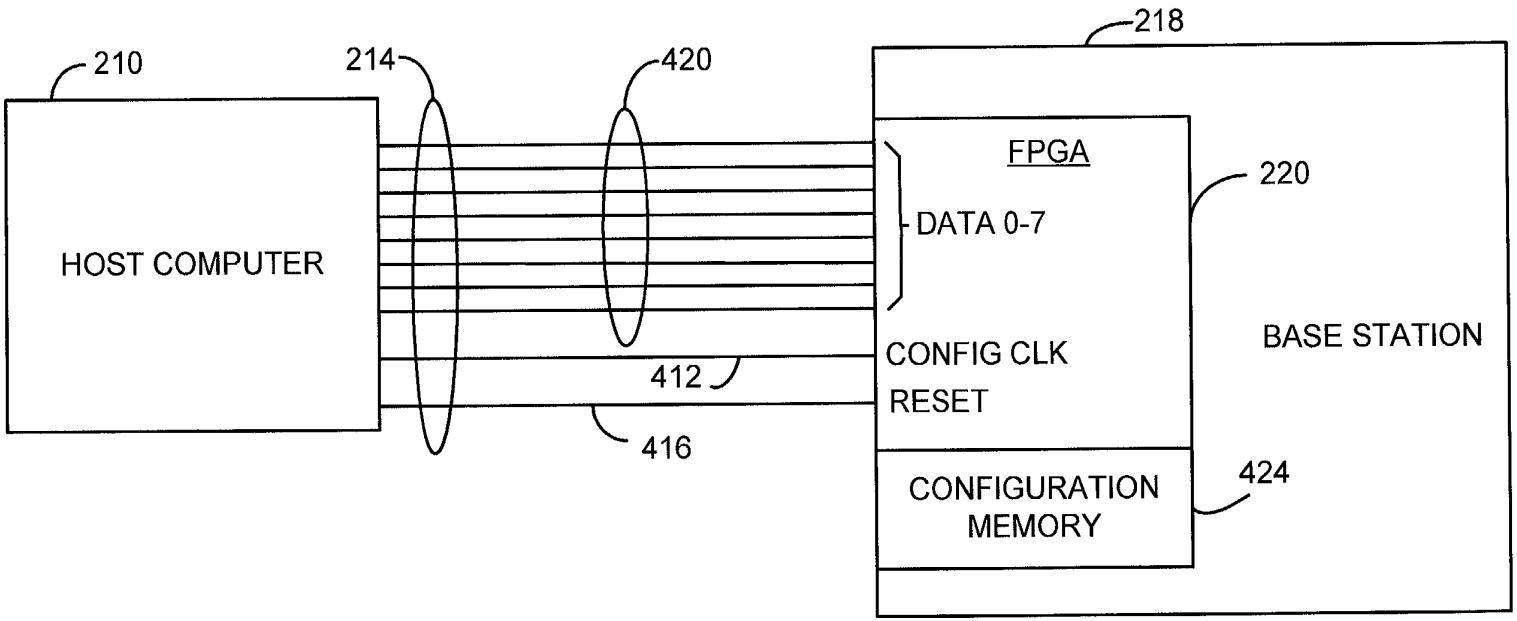


FIG. 6

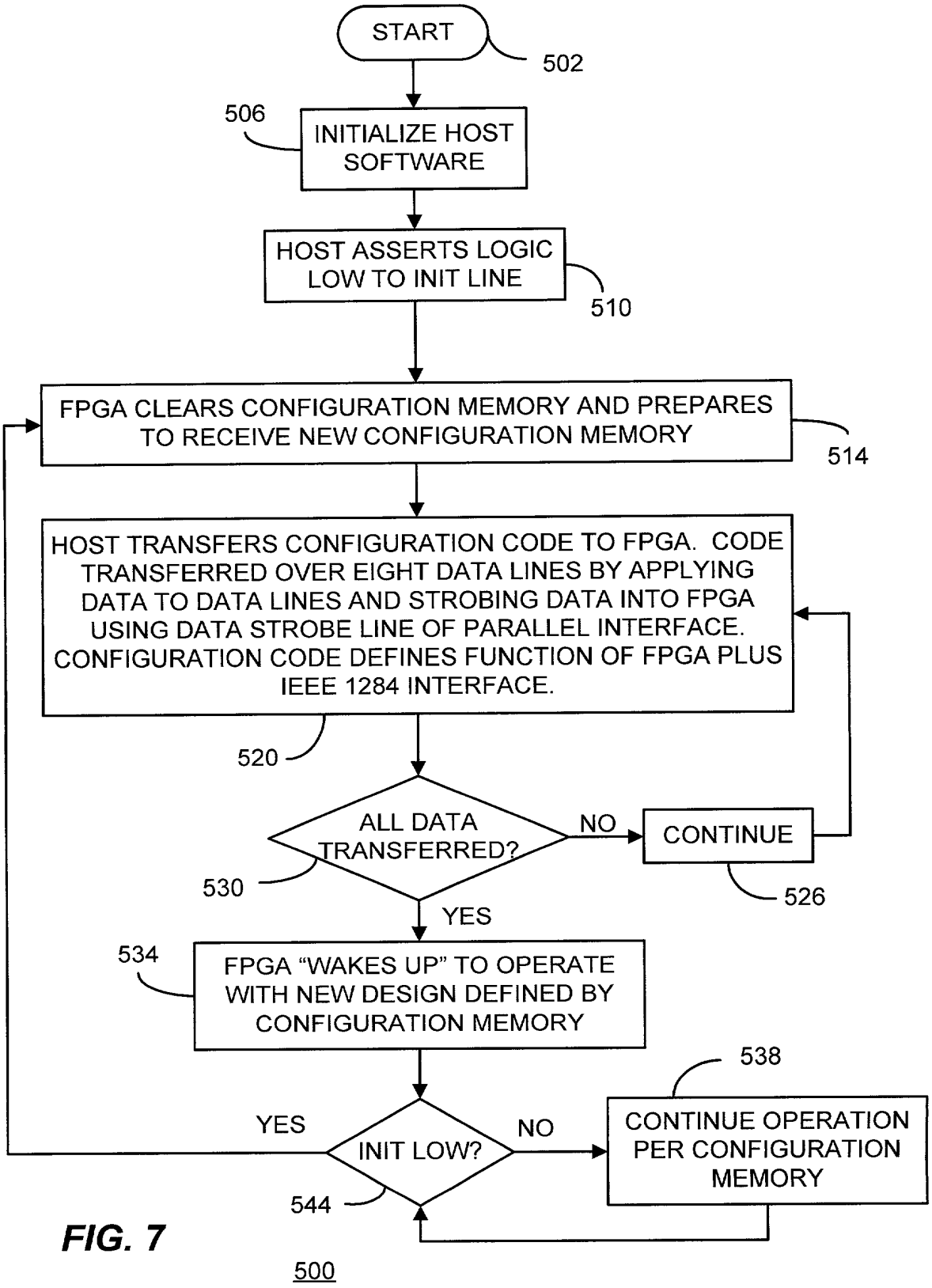

START
502
506
INITIALIZE HOST SOFTWARE
HOST ASSERTS LOGIC LOW TO INIT LINE
510
FPGA CLEARS CONFIGURATION MEMORY AND PREPARES TO RECEIVE NEW CONFIGURATION MEMORY
514
HOST TRANSFERS CONFIGURATION CODE TO FPGA. CODE TRANSFERRED OVER EIGHT DATA LINES BY APPLYING DATA TO DATA LINES AND STROBING DATA INTO FPGA USING DATA STROBE LINE OF PARALLEL INTERFACE. CONFIGURATION CODE DEFINES FUNCTION OF FPGA PLUS IEEE 1284 INTERFACE.
520
ALL DATA TRANSFERRED?
NO
CONTINUE
526
530
YES
534
FPGA "WAKES UP" TO OPERATE WITH NEW DESIGN DEFINED BY CONFIGURATION MEMORY
538
YES
INIT LOW?
NO
CONTINUE OPERATION PER CONFIGURATION MEMORY
544

FIG. 7

500

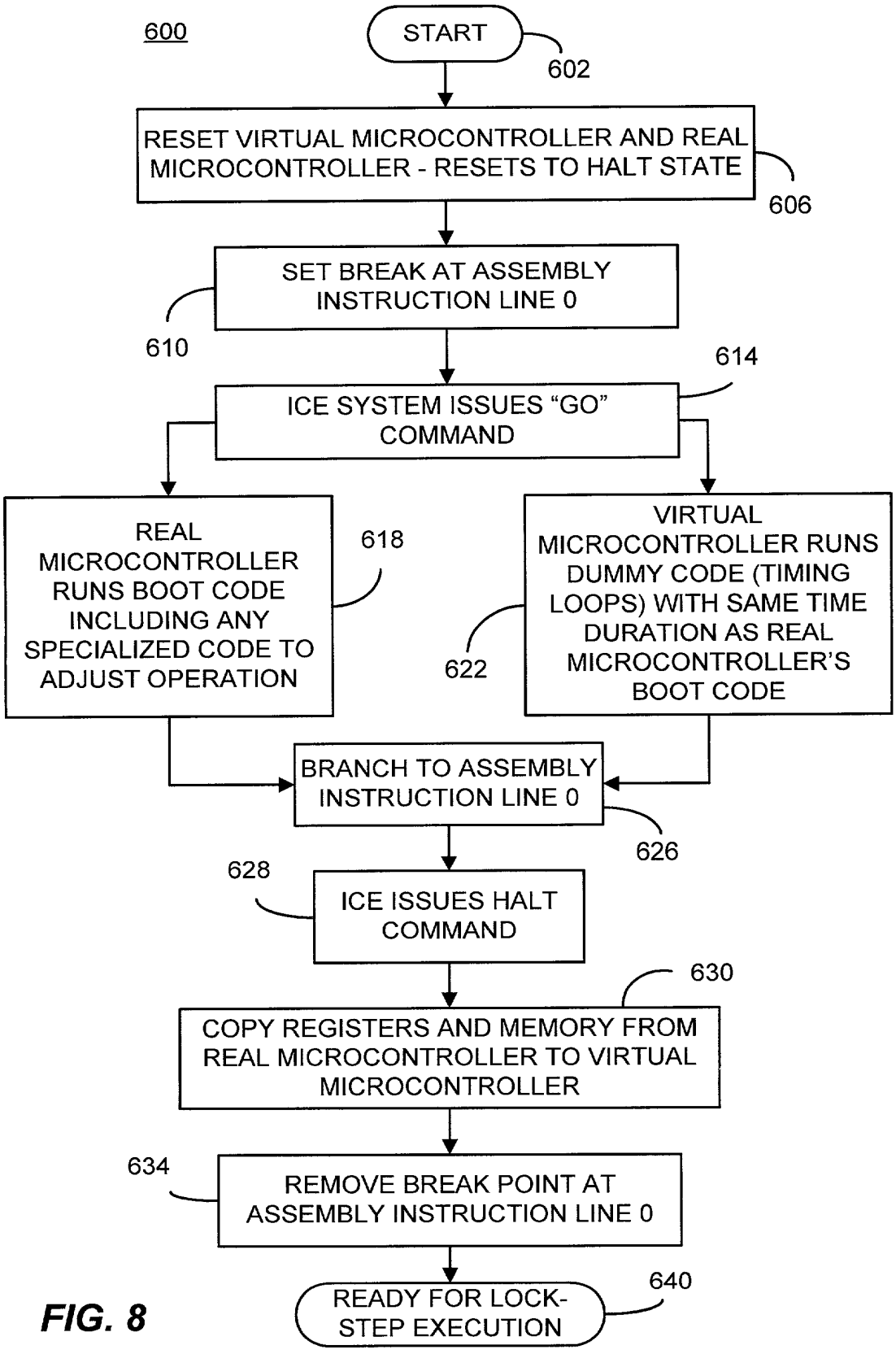

600
START
602
RESET VIRTUAL MICROCONTROLLER AND REAL MICROCONTROLLER - RESETS TO HALT STATE
606
SET BREAK AT ASSEMBLY INSTRUCTION LINE 0
610
614
ICE SYSTEM ISSUES "GO" COMMAND
REAL MICROCONTROLLER RUNS BOOT CODE INCLUDING ANY SPECIALIZED CODE TO ADJUST OPERATION
618
VIRTUAL MICROCONTROLLER RUNS DUMMY CODE (TIMING LOOPS) WITH SAME TIME DURATION AS REAL MICROCONTROLLER'S BOOT CODE
622
BRANCH TO ASSEMBLY INSTRUCTION LINE 0
626
628
ICE ISSUES HALT COMMAND
630
COPY REGISTERS AND MEMORY FROM REAL MICROCONTROLLER TO VIRTUAL MICROCONTROLLER
634
REMOVE BREAK POINT AT ASSEMBLY INSTRUCTION LINE 0
640
READY FOR LOCK-STEP EXECUTION

FIG. 8